Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, APRIL-MAY 2025

Third Semester

Electronics and Communication Engineering

EC3352 - Digital Systems Design

Regulations – 2021

Duration : 3 Hrs ***Maximum : 100 Marks***

PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Convert the hexadecimal number $(B3.2A)_{16}$ into decimal number.	UN	1	2
2.	Simplify the expression Y= A+ AB + A' + B.	UN	1	2
3.	Differentiate between combinational and sequential circuits.	UN	2	2
4.	Realize 2 to 4 line decoder using logic gates.	UN	2	2
5.	Write the characteristic table and characteristic equation of JK Flip flop.	RE	3	2
6.	Draw a 4 bit ring counter with asynchronous inputs.	UN	3	2
7.	What is meant by stable and unstable states in asynchronous circuits?	RE	4	2
8.	List the different modes of asynchronous circuits.	RE	4	2
9.	Define : Noise Margin.	RE	5	2
10.	Compare EPROM and EEPROM.	UN	5	2

PART – B (ANSWER ALL QUESTIONS) (Marks 5*16 = 80)

Q.No			*Questions*	*BLT*	*CO*	*Marks*
11.	a	i	Convert the expression Y = A+BC'+AB+A'BC into canonical form.	L2	1	8
		ii	Express the Boolean function F= XY + X'Z in a product of max terms.	L2	1	8
			Or			
	b	i	Minimize the following logic function using K-map and realize using NAND and NOR gates. F(A,B,C,D) = ∑m(1,3,5,8,9,11,15)+d(2,13).	L2	1	8
		ii	Prove the Demorgan's theorem using truth table.	L2	1	8
12.	a	i	Design and implement a full adder circuit using basic gates.	L3	2	8
		ii	Construct 8: 1 multiplexer using basic gates and implement the function f(x,y,z)= ∑ m(0,2,3,5,7) using multiplexer.	L3	2	8
			Or			
	b		Design a magnitude comparator to compare two numbers where, A= A_1A_0 and B= B_1B_0.	L3	2	16

13.	a	Design a 3 -bit up/ down using JK Flip flop where the input x=1 for up counting and x= 0 for down counting.	L3	3	16
		Or			
	b	Design a four bit universal shift register with function table and explain its operation.	L3	3	16
14.	a	Define races in asynchronous circuits. Illustrate critical and non critical race with an example.	L2	4	16
		Or			
	b	What is a hazard? What are the different types of hazards? Check the circuit with expression $Y = X_1X_2 + X_2' X_3$ has hazard or not. If hazard presents demonstrate its removal.	L2	4	16
15.	a	Compare and contrast the characteristics of TTL, ECL and CMOS logic families.	L3	5	16
		Or			
	b	A combinational circuit is defined by the functions F1 = $\sum$ m(3,5,7) and F2 = $\sum$m(4,5,7). Implement the circuit with PROM and PLA. And analyze the number of gates needed for implementing the function in both the models.	L3	5	16